ABSTRACT OF THE DISCLOSURE

A semiconductor die and an associated low resistance interconnect located primarily on the bottom surface of such die is disclosed. This arrangement provides a flexible packaging structure permitting easy interconnected with other integrated circuits; in this manner, a number of such circuits can be stacked to create high circuit density multi-chip modules. A process for making the device is further disclosed. To preserve structural integrity of a wafer containing such die during manufacturing, a through-hole via formed as part of the interconnect is filled with an inert material during operations associated with subsequent active device formation on such die.